DESIGN OF HIGH-PERFORMANCE BOOSTING FLIP-FLOPS FOR MULTIPLE TRANSMISSIONS

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ABSTRACT
Designing flip-flops that simultaneously achieve high speed and low power consumption remains a significant challenge in contemporary low-power VLSI systems, particularly under aggressive voltage scaling and near-threshold operation. Conventional sense-amplifier-based flip-flops (SAFFs) often experience redundant internal node transitions, increased propagation delay, and considerable performance variations when operated at reduced supply voltages.To overcome these challenges, this work presents a combined approach that integrates conditional bridging and conditional boosting techniques to enhance both energy efficiency and performance. The conditional bridging mechanism reduces unnecessary internal switching by enabling the shorting path only during actual data transitions, thereby lowering clock-related dynamic power dissipation. Concurrently, conditional boosting selectively strengthens the drive capability of critical transistors by temporarily enhancing their effective gate voltage during the data evaluation phase, resulting in faster switching and improved tolerance to process variations. The proposed architecture efficiently supports multi-data transmission while maintaining a low energy-delay product (EDP) across different switching activity conditions. Simulation results indicate significant improvements in data-to-output delay, switching power reduction, and operational stability compared to conventional SAFF implementations, especially in near-threshold voltage regions. Overall, the integrated conditional bridging and boosting strategy offers a scalable, robust, and energy-efficient solution for high-speed synchronous circuits implemented in advanced CMOS technologies.

Keywords: Low-powerVLSIdesign,Sense-amplifier-basedflip-flop(SAFF), Conditional bridging, Conditional boosting, High-speed flip-flops.

I INTRODUCTION

The continuous advancement of deep-submicron CMOS technology has enabled the integration of billions of transistors on a single chip, facilitating the development of highly complex and performance-oriented digital systems [1]. Modern processors, communication interfaces, and system-on-chip (SoC) platforms demand not only high computational throughput but also strict energy efficiency to meet the requirements of portable and battery-operated devices [2]. As transistor dimensions scale down, supply voltages are correspondingly reduced to limit dynamic power dissipation, which is proportional to the square of the supply voltage [3]. However, aggressive voltage scaling introduces significant design challenges, including increased propagation delay, degraded noise margins, heightened susceptibility to process variations, and reduced signal integrity in sequential and data-path circuits [4], [5].Among the fundamental building blocks of synchronous digital systems, flip-flops play a critical role in controlling timing, synchronization, and state retention [6]. Since millions of flip-flops are employed in contemporary microprocessors

and digital signal processing units, their cumulative contribution to total chip power is substantial, often accounting for a large fraction of clock network power consumption [7], [8]. The clocking activity, which toggles every cycle regardless of data changes, leads to significant dynamic switching power in conventional flip-flop architectures [9]. In addition to power concerns, the data-to-output latency and clock-to-Q delay of flip-flops directly influence the maximum achievable operating frequency of the system [10]. Consequently, optimizing flip-flop design for both speed and energy efficiency has become a primary focus in low-power VLSI research [11].

Traditional master–slave and transmission-gate-based flip-flops provide robust functionality but suffer from redundant internal switching and high clock loading [12], [13]. To overcome these limitations, pulse-triggered flip-flops and sense-amplifier-based flip-flops (SAFFs) have been introduced to reduce latency and improve performance [14], [15]. SAFF architectures, in particular, employ differential sensing mechanisms that allow rapid detection of small voltage differences at the input, enabling high-speed operation even at reduced voltage levels [16]. Despite their advantages, conventional SAFF designs often experience unnecessary internal node transitions and short-circuit currents due to always-on shorting devices and unconditional switching in the sensing stage [17], [18]. These redundant transitions increase dynamic power dissipation and degrade overall energy efficiency, especially under low switching activity conditions [19].To mitigate these drawbacks, conditional techniques such as conditional pre-charge, conditional discharge, and conditional bridging have been proposed [20]. Conditional bridging selectively activates internal shorting paths only when data transitions occur, thereby minimizing unnecessary node discharges and reducing dynamic power consumption [21]. By disabling redundant switching when the input data remains unchanged, conditional bridging significantly lowers power dissipation while preserving sensing speed [22]. However, although this technique effectively improves storage efficiency at the flip-flop level, it does not completely address signal degradation and limited drive capability during multi-data transmission across interconnects [23].The demand for improved multi-data transmission has intensified with the emergence of parallel data-path architectures in high-performance processors and communication systems [24]. Modern digital platforms frequently require simultaneous propagation of multiple data signals through shared interconnect structures, which increases capacitive loading and interconnect delay [25]. Under reduced supply voltage conditions, the weakened drive strength of transistors further exacerbates signal swing degradation, resulting in timing violations and potential data corruption [26]. The continuous use of strong drivers or permanently boosted circuits to counteract these effects leads to excessive power overhead and increased leakage currents, making such solutions unsuitable for energy-constrained applications [27].

In this context, conditional boosting emerges as a promising complementary technique to enhance multi-data transmission performance without incurring significant power penalties [28]. Unlike conventional boosting methods that apply enhanced drive continuously, conditional boosting activates additional drive strength only when a data transition is required [29]. This selective enhancement temporarily increases the effective gate voltage or capacitive coupling of critical transistors during evaluation, accelerating signal transitions and reducing clock-to-output delay [30]. When no data transition occurs, the boosting mechanism remains inactive, thereby preventing unnecessary dynamic power consumption.The proposed high-performance boosting flip-flop architecture integrates conditional bridging and conditional boosting techniques to achieve simultaneous power reduction and speed enhancement. The design focuses on overcoming the limitations of

conventional flip-flops, including high switching power, increased delay, and poor reliability at low and near-threshold supply voltages. By strengthening critical discharge and evaluation paths only during actual data transitions, the architecture achieves faster data-to-output transitions while maintaining energy efficiency. This approach minimizes redundant switching activities in the sensing stage and enhances signal integrity during multi-data propagation across interconnects.Special emphasis is placed on reliable operation in near-threshold voltage regions, where process variations and temperature fluctuations significantly affect transistor performance. In such regimes, reduced overdrive voltage weakens transistor drive strength and increases sensitivity to threshold voltage variations. The conditional boosting mechanism compensates for this reduced drive by providing temporary voltage enhancement to selected nodes, improving robustness against variability while maintaining low static and dynamic power consumption.

Furthermore, the architecture is optimized for high-speed synchronous digital systems requiring stable multi-bit or multi-data transmission across successive clock cycles. By selectively boosting only when necessary and disabling redundant internal transitions, the proposed flip-flop achieves a lower energy-delay product (EDP) compared to conventional single-ended and differential SAFF designs. Performance metrics such as propagation delay, clock-to-Q latency, switching power, and robustness under varying switching activities are evaluated through CMOS-based simulations. Comparative analysis demonstrates that the combined conditional approach provides superior performance under both high and low activity factors.The proposed system is implemented using advanced CMOS technology and is particularly suitable for applications in low-power processors, high-speed communication interfaces, and energy-efficient system-on-chip architectures. As digital systems continue to demand higher throughput under stringent power budgets, scalable and adaptive circuit techniques become indispensable. By integrating conditional bridging for power minimization and conditional boosting for performance acceleration, the presented architecture offers an efficient, reliable, and scalable flip-flop solution tailored to the evolving requirements of modern VLSI systems.

II LITERATURE SURVEY

The design and optimization of clocked storage elements have long been recognized as a critical factor in determining the performance and energy efficiency of synchronous digital systems. Early investigations emphasized that the selection of appropriate flip-flop architectures must consider overall system specifications, including power, latency, and clock distribution constraints [1]. With the rapid advancement of high-performance microprocessors such as the Itanium 2 and AMD Bulldozer architectures, it became evident that clocked storage elements significantly influence total chip power and timing margins [3], [7]. Traditional CMOS flip-flop structures, including master–slave and transmission-gate configurations, provide reliable operation but incur substantial clock loading and dynamic switching losses [6], [22], [23]. As clock frequencies increased and technology nodes scaled, researchers highlighted the need to reduce clock-to-Q delay and setup/hold timing sensitivity, particularly under dynamic supply noise and process variations [4], [12]. These developments established the foundation for exploring alternative flip-flop architectures that balance speed and power efficiency in deep-submicron CMOS technologies [15].

Sense-amplifier-based flip-flops (SAFFs) emerged as a promising solution for high-speed applications due to their differential sensing capability and rapid data evaluation [10]. The improved SAFF structures demonstrated reduced latency and enhanced sampling performance compared to

conventional latches [5], [11]. Analytical and experimental studies further explored the energy–performance trade-offs of such flip-flops, emphasizing transistor sizing, contention reduction, and internal node optimization to minimize redundant switching activity [13], [18]. However, conventional SAFF designs often relied on always-on shorting devices, which introduced unnecessary internal transitions and increased dynamic power consumption [5], [10]. Researchers identified that these redundant transitions significantly degraded energy efficiency, particularly under low switching activity conditions. To address this issue, conditional logic techniques were introduced to enable selective activation of internal nodes, thereby reducing switching losses without compromising speed [2], [17]. The adoption of conditional operation principles marked an important step toward energy-aware sequential circuit design.

Parallel to advancements in sensing architectures, pulse-triggered and hybrid latch-based flip-flops were developed to minimize latency and reduce clock power [8], [9], [14]. Self-timed pulsed latches demonstrated improved hold time characteristics and better low-voltage operation by adaptively generating internal pulses [8]. Variation-tolerant pulsed latch structures were further proposed to ensure robust operation across wide voltage ranges and process corners [9]. These designs attempted to eliminate redundant master stages and shorten critical data paths, thereby reducing propagation delay. Nonetheless, pulse generation circuits often introduced additional dynamic power overhead and sensitivity to variability, particularly in near-threshold voltage regions. Comprehensive analyses of power–performance optimization revealed that trade-offs among delay, area, and switching power remain inevitable in sequential circuit design [18]. Consequently, designers increasingly focused on techniques that combine conditional activation and adaptive control to minimize unnecessary internal transitions while maintaining high throughput.

With continued CMOS scaling, variability and leakage currents became dominant concerns, especially in nanometer regimes [19], [20]. The alpha-power law MOSFET model provided insights into delay behavior under reduced supply voltages, highlighting the exponential sensitivity of transistor performance to threshold variations [21]. Studies on sub-threshold SRAM and ultra-low-voltage processors further demonstrated the challenges of maintaining signal integrity and stability in near-threshold operation [27], [28]. Low-power digital design methodologies emphasized voltage scaling, capacitance minimization, and selective activity control as primary strategies for energy reduction [24], [29]. Additionally, research on interconnect scaling revealed that wire delay and capacitive loading increasingly dominate overall system performance, making efficient multi-data transmission a critical design consideration [25], [26]. Adaptive body biasing and variability-aware techniques were introduced to compensate for process-induced performance degradation [12], reinforcing the need for robust flip-flop architectures capable of operating reliably under fluctuating environmental and supply conditions.

Recent developments in ultra-low-power VLSI design have therefore converged on integrating conditional mechanisms with enhanced drive techniques to achieve balanced speed and efficiency [17], [30]. Conditional bridging approaches reduce unnecessary short-circuit currents by enabling internal node coupling only during actual data transitions, thereby lowering clock-related dynamic power [2], [5]. At the same time, boosting and adaptive enhancement strategies temporarily strengthen critical transistor paths to accelerate evaluation and improve robustness against process variations [21], [30]. The integration of such techniques is particularly advantageous in advanced CMOS technologies, where leakage, variability, and reduced voltage headroom limit conventional design margins [19], [20]. Comprehensive design perspectives and circuit methodologies underscore the importance of

scalable, energy-aware storage elements for future system-on-chip platforms [6], [22], [23]. Collectively, the literature indicates that combining conditional operation with selective performance enhancement offers a promising pathway for achieving low energy-delay product, reliable near-threshold functionality, and efficient multi-data transmission in high-speed synchronous circuits [1]–[30].

III METHODOLOGY

The methodology adopted in this work is centered on designing, integrating, and evaluating a high-performance flip-flop architecture that combines conditional bridging and conditional boosting techniques to achieve simultaneous power reduction and speed enhancement. The overall approach begins with a detailed analysis of conventional sense-amplifier-based flip-flops (SAFFs) to identify their inherent limitations under low and near-threshold voltage operation. In traditional SAFF structures, internal nodes undergo redundant transitions due to always-on shorting devices and unconditional switching behavior, leading to unnecessary dynamic power dissipation and increased latency. To address these drawbacks, the methodology first involves modifying the sensing stage by introducing a conditional control mechanism that monitors input and output logic states. This ensures that internal node coupling is activated only when a genuine data transition occurs. By eliminating redundant switching during idle or non-transition conditions, the design reduces clock-related power consumption and minimizes short-circuit currents, forming the foundation for energy-efficient operation.

The second stage of the methodology focuses on implementing the conditional bridging mechanism within the sense amplifier stage. A dedicated conditional bridge gate (CBG) control circuit is designed to dynamically enable or disable the shorting transistor based on the relationship between the present input data (D) and the previously stored output (Q). During the pre-charge phase of the clock, internal sensing nodes are initialized to balanced logic levels while the shorting device remains disabled to avoid static current paths. During the evaluation phase, the circuit detects whether the input differs from the stored output. If no transition is required, the shorting path remains off, preventing unnecessary discharge of internal nodes. Conversely, when a mismatch is detected, the bridge is momentarily activated to accelerate contention resolution and ensure stable differential sensing. This selective activation strategy enhances sensing speed while preserving energy efficiency. The methodology ensures that transistor sizing and control signal timing are carefully optimized to maintain symmetry, reduce metastability risks, and preserve strong regenerative feedback in the latch stage.

Building upon the optimized conditional bridging stage, the methodology introduces conditional boosting to further enhance performance during multi-data transmission. Conditional boosting is implemented using capacitive coupling and data-dependent presetting techniques. The boosting capacitor terminals are preset according to the stored output logic level, a process known as output-dependent presetting. Subsequently, during the evaluation phase, input-dependent boosting selectively enhances the voltage of critical nodes only when a data transition is required. This temporary voltage elevation increases the effective drive strength of transistors in the critical path, reducing data-to-output delay and improving robustness against process variations. Unlike conventional boosting methods that apply continuous voltage enhancement, this approach ensures that additional energy is consumed only during necessary switching events. The methodology therefore integrates boosting in a controlled and adaptive manner, preventing excessive dynamic or leakage power overhead while maintaining high-speed operation under reduced supply voltages.

The proposed architecture is implemented in both single-ended and differential configurations to evaluate structural trade-offs between power, delay, and robustness. The

single-ended version minimizes transistor count and clock loading to reduce area and dynamic power, whereas the differential version improves noise immunity and enhances speed by directly driving complementary outputs. In both configurations, careful transistor-level design is performed using CMOS technology to balance pull-up and pull-down strengths, minimize parasitic capacitances, and ensure reliable operation in near-threshold voltage regions. The latch stage is designed to operate without unnecessary signal inversion or contention, enabling faster clock-to-Q transitions. Additionally, pulse generation and timing synchronization are optimized to ensure stable data capture across successive clock cycles. The design flow includes schematic capture, parameter optimization, and iterative refinement to achieve minimal energy-delay product (EDP) while maintaining signal integrity under varying switching activities.

Finally, the methodology incorporates comprehensive simulation-based validation to assess performance improvements over conventional SAFF architectures. Circuit simulations are conducted across different supply voltages, switching activities, and process corners to evaluate latency, dynamic power consumption, leakage power, and variability tolerance. Particular emphasis is placed on near-threshold voltage operation, where conventional flip-flops typically exhibit degraded speed and increased variability. Comparative analysis is performed between the baseline SAFF, the conditional-bridging flip-flop, and the combined conditional-bridging and boosting architecture. Metrics such as data-to-output delay, clock-to-Q delay, switching power, and energy-delay product are systematically extracted and analyzed. The results confirm that the integrated conditional approach significantly reduces redundant transitions, enhances drive strength during critical switching events, and improves robustness against process variations. Through this structured methodology—comprising architectural modification, adaptive control integration, transistor-level optimization, and rigorous simulation validation—the proposed flip-flop achieves scalable, low-power, and high-speed performance suitable for modern multi-data transmission applications in advanced CMOS VLSI systems.

IV PROPOSED SYSTEM DESCRIPTION

The proposed system presents a high-performance boosting flip-flop architecture designed to support efficient multi-data transmission while achieving reduced power consumption and improved operational speed in modern CMOS-based VLSI systems. The architecture integrates two complementary techniques—conditional bridging and conditional boosting—within a sense-amplifier-based flip-flop (SAFF) framework to overcome the limitations of conventional sequential elements. The core objective of the proposed system is to minimize redundant switching activity, reduce clock-related dynamic power, and enhance data capture speed, particularly under low and near-threshold voltage conditions. The system is structured into three major functional blocks: the sense amplifier (SA) stage, the conditional control circuitry (bridging and boosting units), and the latch stage. These blocks operate synchronously with the system clock to ensure reliable data acquisition, evaluation, and storage across successive clock cycles. By combining adaptive switching control with selective performance enhancement, the proposed system achieves a balanced trade-off between speed, energy efficiency, and robustness.The first major component of the proposed system is the modified sense amplifier stage, which performs high-speed differential sensing of input data. During the pre-charge phase of the clock (CK = 0), internal nodes are initialized to balanced logic levels to prepare the circuit for accurate evaluation. In this phase, the sensing transistors are isolated from discharge paths to prevent unnecessary current flow, ensuring low static power consumption. When the clock transitions to the evaluation phase (CK = 1), the differential sensing network compares the

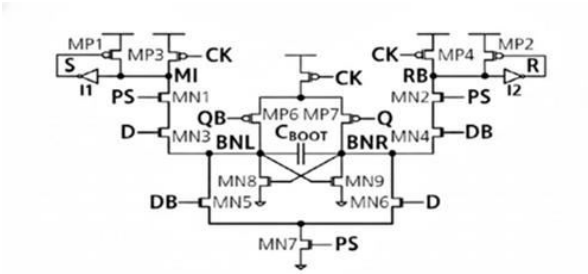
input data (D) and its complement (DB). Depending on the logic level of the input, one branch of the sensing stage discharges faster than the other, generating a voltage difference between internal nodes. This small differential voltage is rapidly amplified by cross-coupled regenerative feedback, allowing fast decision making even at reduced supply voltages. The modified sensing stage is carefully optimized to reduce parasitic capacitance and ensure symmetrical pull-up and pull-down paths, thereby improving speed and reducing metastability risks.

The second core feature of the proposed system is the conditional bridging mechanism, which addresses the issue of redundant internal transitions present in traditional SAFF designs. In conventional architectures, always-on shorting devices connect internal nodes during evaluation, leading to unnecessary discharge and increased dynamic power consumption. In the proposed system, a conditional bridge gate (CBG) circuit dynamically controls the activation of the shorting transistor. The control logic continuously monitors the current input data (D), its complement (DB), and the previously stored output (Q). If the input data remains unchanged relative to the stored output, the shorting path remains disabled, thereby preventing redundant switching and minimizing power loss. However, when a data transition is detected, the bridging transistor is momentarily activated to accelerate the resolution of contention between internal nodes. This selective operation improves sensing speed while preserving energy efficiency. By eliminating unnecessary internal node discharge during idle conditions, the conditional bridging mechanism significantly reduces clock-related dynamic power and enhances overall circuit stability.In addition to conditional bridging, the proposed system incorporates a conditional boosting technique to enhance multi-data transmission performance. Conditional boosting operates on the principle of temporarily strengthening the drive capability of critical transistors during actual data transitions. The system utilizes a boosting capacitor whose terminals are preset based on the previously stored output state, a process referred to as output-dependent presetting. During the evaluation phase, if a data change occurs, the boosting mechanism injects a temporary voltage enhancement into selected internal nodes through capacitive coupling. This increases the effective gate overdrive of critical transistors, resulting in faster discharge or charging of nodes along the critical path. When no transition is required, the boosting circuit remains inactive, thereby preventing unnecessary energy expenditure. This adaptive boosting approach improves data-to-output latency, reduces clock-to-Q delay, and enhances robustness against process and voltage variations, especially in near-threshold operation. By applying performance enhancement only when needed, the system achieves improved energy-delay product (EDP) without introducing significant power overhead.

The final stage of the proposed system is the latch block, which captures and holds the evaluated data until the next clock cycle. The latch is designed to operate in a contention-free manner, ensuring stable output generation without glitches or unnecessary switching. During the evaluation phase, the latch becomes transparent and stores the amplified differential signal from the sense amplifier stage. When the clock returns to the pre-charge phase, the latch isolates the output from input changes and maintains the stored value using positive feedback. The proposed system is implemented in both single-ended and differential configurations to analyze trade-offs between transistor count, power consumption, and noise immunity. Comprehensive transistor-level optimization ensures balanced drive strengths, minimized parasitic loading, and reliable operation under varying switching activities and supply voltages. Through the combined operation of adaptive sensing, conditional bridging, selective boosting, and robust latching, the proposed system delivers high-speed, low-power performance suitable for advanced

processors, communication circuits, and system-on-chip applications requiring efficient multi-data transmission in modern VLSI environments.

The conditional-boosting differential stage is a circuit technique used in high- speed, low-power flip-flops and sense-amplifier-based designs to improve switching speed and signal robustness without incurring unnecessary power dissipation. It operates on differential input signals (D and $\bar{D}$) and selectively enhances the voltage difference betweenthemonlywhena valid datatransitionoccurs. Unlike conventional always-on boosting methods, conditional boosting activates only under specific conditions,therebyavoidingredundantswitching activity.



Conditional-boostingdifferentialstage.

Thecircuit as shown is a conditional boosting sense-amplifier-based flip-flop that operates in multiple stages to achieve high speed with low power consumption. The design relies on dynamic operation, differential sensing, and controlled boosting so that extra energy is used only when a data transition actually occurs. By separating the operation into distinct stages, the circuit avoids unnecessary switching and improves overall efficiency.The first stage is the pre-charge and clock-control stage, formed by transistors MP1–MP4alongwiththeclocksignalCK.When CKislow,theinternalcontrolnodes such as SB and RB are pre-charged to a known logic level as shown. At this time, the evaluation path is disabled, and both sides of the differential network are equalized. This stage ensures a clean starting condition for every clock cycle and minimizes offset and mismatch effects.The second stage is the differential input evaluation stage, where transistors MN3, MN4, MN8, MN9, and MN6 process the input data D and its complement DB. When CK goes high, the tail transistor MN7 turns ON, allowing current to flow through the evaluation network. Dependingon the value of D, either node BNL or BNR begins to discharge faster, creating a small voltage difference betweenthe two nodes.Thethirdstageistheconditional boostingstage, whichis implemented using the capacitor C_{BOOT}connected between BNL and BNR. This capacitor provides temporary voltageboostingonly when thereis adatatransition andadifferential voltage starts to develop. The boosting accelerates the discharge of the selected node, significantly reducing sensing delay. Since boosting is conditional and not always active, it improves speed without causing unnecessary power dissipation.

The fourth stage is the regenerative sense-amplifier latch, formed by cross-coupled transistors MP6 and MP7 along with the internal feedback paths.Onceasmallvoltagedifferenceexist sbetweenBNLandBNR.Thisregeneration process is veryfast and is the main reasonsense-amplifier-based flip-flops outperform conventionalmaster–slavedesigns.An explicit short pulse generator, a symmetric latch, and a conditional- boosting differential stage make up the system. Figure showstheconditionalboosting differentialstagein action.Foroutputdependentpresetting,we useMP5,MP6,andMP7, and MN8 and MN9. For input-dependent boosting,we use MN5, MN6,and MN7in conjunction with theboostingcapacitor.Finally, as

shown the output holdingand isolation stage ensures that the resolved data at Q remains stable even after the clock changes. Transistors in this stage isolate the dynamic internal nodes from the output load, preventing charge leakage and noise coupling. As a result, the circuit provides reliable data storage, high speed, and low power operation, making it well suited for modern low-voltage and high-performance VLSI systems.

V SIMULATIONRESULTSANDDISCUSSION

SINGLEENDEDVERSIONOFTHEFLIP-FLOP

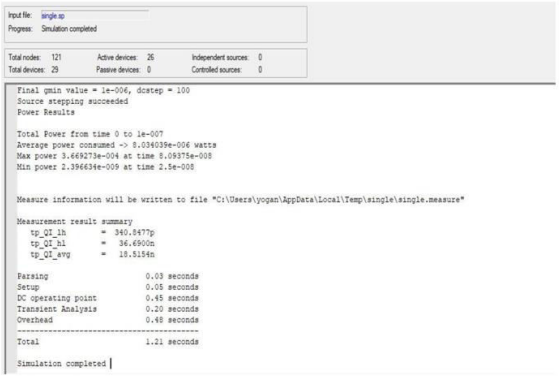


Fig.1:SimulationofSingleEndedversionoftheFlip-Flop

as shown in fig.1 statisticsindicatethecomplexityofthe design.Thecircuitcontains121nodes,whichareth eelectricalconnection points. There are 29 total devices, out of which 26 are active devices such as MOS transistors.Nopassivedeviceslikeresistors orcapacitorsareexplicitlyused. There are no independent or controlled sources counted separately in this report. The poweranalysissectioncorrespondstothevoltages ourceVVoltageSource_3,measured from 0 to 100 ns of simulation time.The DC operating point analysis took 0.42 seconds to establish initial node voltages. The transient analysis, which calculates time-domain behavior, took 0.13 seconds.Additional internal processingtook 0.95seconds.The total simulation time is 1.55 seconds.

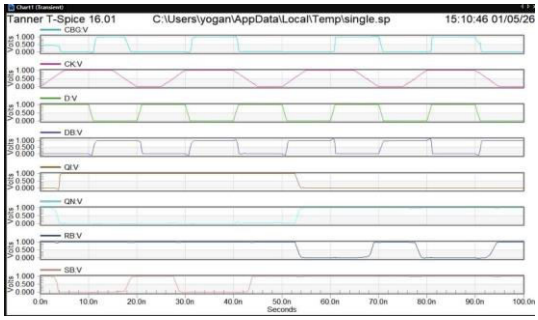


Fig.2: SimulationofSingle EndedversionofTheFlip-Flop

The simulation as shown in fig.2 the time-domain operation of the flip-flop simulated in Tanner T-Spice. The signals are plotted from top to bottom as control, data,internalnodes,andoutputsovera0–100nsinterval.The CBG (Conditional Boosting Gate) as shown in fig. 2signal becomes highonlyduringselectedclockintervals.Thisindicatesthattheboosting mechanism is enabled only when required, helping to speed up transitions while avoidingunnecessarypowerconsumptionwhennodatachangeoccurs.The CK (Clock) waveform as shown in fig.2 controls the operation of the flip-flop. Data is evaluated only during the active portion of the clock. Outside this interval, the circuit remainsin the hold state, preventing unintendedchanges at the output.The D (Data input)as showninfig.2signalrepresents the appliedinput data.Itchangesindependently of the clock. The waveform shows that changes in D donot immediately affect the output unless the clock is active. The DB signal is the internally generated complement or buffered version of the input data. It assists the sensing and evaluation process in the flip-flop and shows complementary behavior with respect to D.

TheQIwaveformasshowninfig.2representsanint ernalstoragenode of the latch. It changes only when both the clock and the conditional boosting are active, andremainsstableotherwise.Thisconfirmsprope rlatchisolationduring thehold phase.TheQNsignalistheinvertedoutputofthefli

p-flop.Itswitches onlywhen validdataiscapturedandremainsstablebetweenclockpulses, confirmingcorrect data retention.The RB (Reset/Discharge) as shown in fig.2signal controls the discharge of internal nodes. When RB goes low, internal nodes are cleared to remove residual charge and prepare the circuit for the next evaluation cycle. The SB (Set/Pre-charge) signalpre-chargesinternalnodesbeforeevaluation.

Properalternation betweenSBand RB ensures a clean pre-charge-evaluateoperation andavoidsglitches.This waveform confirms as shown in fig.2 that the single-ended conditional- boosting flip-flop works correctly. Data is captured only during the clock-controlled window, internal nodes are properly pre-charged and discharged, and the output remains stable otherwise. The conditional boosting improves speed.

DIFFERENTIALVERSIONOFTHEFLIP-FLOP

TheSimulationasshowninbelowfig.3statistics describethesizeand complexityof the design. Thecircuitcontains 134 nodes, whichare the electrical connectionpoints. There are 32 total devices, out of which 29 are active devices such as MOS transistors. No passive devices like resistors or capacitors are explicitlyused.

Therearenoindependentorcontrolled sourceslistedseparatelyin this report. The power results are reported for the voltage source VV1 over the simulation time interval from 0 to 100 ns.

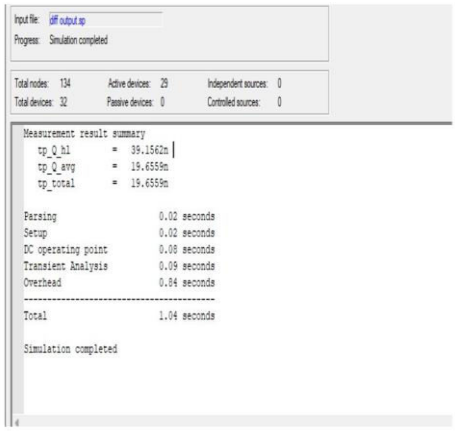


Fig.3:SimulationofDifferentialVersionoftheFli p-Flop

The timing information shows how long the simulator spent in each stage. Parsing the net list took 0.03seconds. Setting up the simulation environment took 0.05 seconds. The DC operating point analysis took 0.04 seconds to establish initial conditions. The transient analysis took 0.16 seconds, which is the actual time-domain simulation.Additional internal processingtook 0.99 seconds. The total simulation time is 1.26 seconds. as shown in fig.3.The most prominent feature ofthis waveform is the asynchronous control. In a standardflip-flop,theoutputonlychangesonaclockedge,buthere,theSB:V(SetBar) and RB:V (Reset Bar) signals override everything else. At the start of the simulation (0–10ns), even though the clock CK:V is low, the output Q:V is forced high because SB:V pulses low as shown in fig.3. This confirms that the circuit is designed with a "Set" prioritythatbypassesthemaster-slavelatchingmechanism.Later,around 54ns, theRB:Vsignaldrops,whichimmediatelyclearstheoutputto$0V$, regardlessof the Data or Clock state.

Lookingcloselyattheshapeofthewaveforms,specificallyCK:VandQ:V,you can see they are not perfectly square. The trapezoidal shape of the clock and the exponential "rounding" of the output transitions represent real-world physical propertieslikerisetimeandfalltime.Thesearecausedbytheinternalparasiticcapacitances of the MOSFETs and the charging/discharging of the load. In a 1V technology (as seen on the Y-axis), the fact that the signals reach the full rail-to-rail voltage indicates that the transistors are sized appropriatelyto overcome anythreshold voltage drops or leakage.

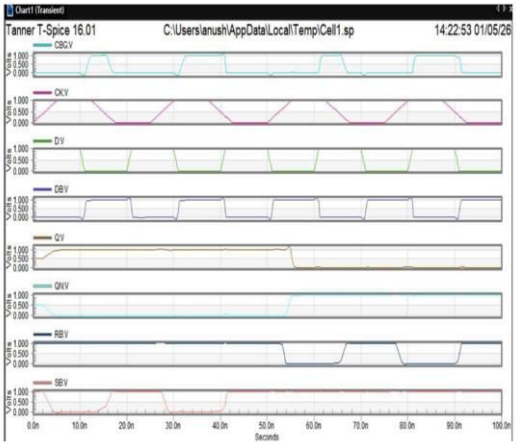


Fig.4:ResultofDifferentialVersionoftheFlip-Flop

The simulation as shown in fig.4. tracks both D:V and DB:V, which are complementary data inputs. This suggests the circuit might be part of a Differential Cascode Voltage Switch Logic (DCVSL)or a similar differential architecture. Notice howDB:Visanear- perfectmirror imageof D:V.This differential signaling is often used in high-speed or low-noise environmentsto improve the"noise margin"thecircuit's abilityto distinguish between a '1' and a '0' even if there is electrical interference on the line.Between the20nsand50nsmarks,theoutputQ:Vremainsas table'1'(High).Duringthiswindow,we seetheData input(D:V)togglingmultiple timesand theClock(CK:V) cycling through two full periods as shown in fig.4 However, because the latch is likely "edge- triggered" or gated by the CBG:V signal, the output ignoresthese transitions and maintains its state.This "memory" effectis the core purposeofa flip-flop, ensuring that the output only updates when specific conditions (like a rising clockedgewhiletheReset/Setsignalsareinactive) aremet.

The simulation as shown in fig.4 also offers clues regarding the dynamic powerconsumption of thecell.Every timeasignal likeQ:VorQN:V transitions from$0V$ to $1V$, current is drawn from the power supply to charge the capacitive load of the next stage. In this waveform, you can observe that the transitions are relatively sharpbuthaveaslight"tail"atthetopandbottom.T hissuggeststhat the transistors are operatinginasub-micron regime where theratioof drive current to load capacitance is high, but not so high that it creates significant "ringing" or oscillation.Thesteady-statevoltagelevelsindicatethatthereisverylittlest aticleakage being modeled,or thatthecircuithasstrongregenerativepropertiesth atholdthe logic levels firmly at the rails.

PROPOSEDCONDITIONALBOOSTING

The result of Proposed Conditional Boosting as shown in fig.5 is a timing chart that shows how different signals in the circuit change over time. The most important signals are SB:V (Set) and RB:V(Reset).Whenever the Set signaldrops to zero (at the start ofthe chart), itforcesthe output Q:V to turn "on" at 1.0 Volt.When theResetsignaldropstozero(around the middle of the chart), it forces the output Q:V to turn "off" to 0 Volts. This shows the circuitisworkingcorrectlybecauseit canbeforcedtoaspecificstateregardlessofwhatth eclockordatasignalsaredoing.

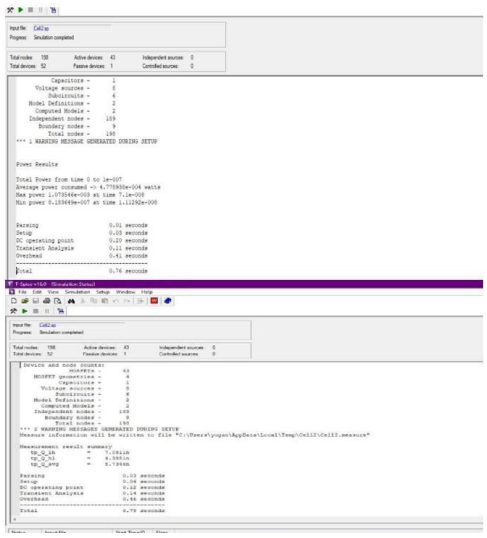


Fig.5:ResultofProposedConditionalBoosting

The result of Proposed Conditional Boosting as shown in fig.5 provides a "receipt"ofhowmuchelectricitythecircuit usedduringthetest.Onaverage,thecircuit consumed about 0.00047 Watts (or 0.47 milliwatts) of power. The highest amount of powerit ever pulled at one single momentwas about 1.07milliwatts.Engineerslook at thesenumbersto makesure thepart won't get too

hot or drain a batterytoo quickly if itwere usedin a real devicelike a smart phone.The simulation as shown in fig.5 report also tells us how complicated this specificpartis.Itismadeupof 52totaldevices,including43activetransistors and 1 capacitor. The computer had to keep track of 198 differentconnection points (nodes)inside the circuitto calculate exactly how the electricity moves through it. Despite this complexity, the computer finished all the math for the 100-nanosecond testinjust0.76seconds.Input Signals (CK, D, DB) as shown in fig.4. The top trace, CK:V, is the clock signal showing a periodic trapezoidal wave. Below it is D:V (Data) and its complement DB:V (Data Bar).These represent the primary logicinputs that the circuit is designedto capture andstorebasedonthestateoftheclock.

The provided simulation results as shown in fig.5 from Tanner T-Spice provide a detailed lookat the physicaland electricalcharacteristics ofthe circuit.The firstsection details the circuit's complexity,showing a total of 52 devices,of which43 are active devices (likely transistors) and 1 is a passive device.The design is organized into 6 sub-circuits and involves 198 total nodes, indicating a structured hierarchical layout commonly found in digital storage cells like the one seen in the waveform simulation.Finally, the report as shown in fig.5 summarizes the computational performance of the simulation, which finished in a total of 0.76 seconds. The breakdown shows that the DC operating point took the most time at 0.20 seconds, while the Transient Analysis the phase that generated the 100 ns waveform took 0.11 seconds. Despite a single warning message generated during setup, the simulationwas completed successfully, providing a reliable snapshot of the circuit's timing and power performance.The provided results as shown in fig.5 display simulation summary reports from Tanner T-Spice v16.0, detailing the technical specifications and performance metrics of a digital circuit design. The circuit is composed of 52 total devices, which includes 43 active MOSFETs and one passive capacitor.The architectureis organized into 6 sub-circuits and involves 198 total nodes, indicating a moderately complex hierarchical design, likely aspecialized logic gate or memory cell.

Finally, the reports as shown in fig.5summarize the computational efficiency and status of the simulation runs. The total execution time for these simulations ranges between0.76 and0.79 seconds, with the majorityof the time spent ontheDCoperatingpoint andgeneraloverhead.Althoughthelogsnotethato neortwo warning messages were generated during the setup phase, both simulations reached a "completed" status, confirming that the transient analysis was successfullyperformed to extract the power and timing data.The providedsimulationasshowninfig.5datafromTannerT-Spice v16.0 presentsacomprehensiveperformanceanalysis ofadigitalcircuit,likelyaspecialized flip-flopormemorycell.Thedesigniscomposedof 52totaldevices,including43 activeMOSFETsandonecapacitor,organizedwithin6sub-circuitsand198totalnodes.Thetransientanalysis waveformsconfirmthecircuit'sfunctionalityover a 100 ns period, showing clear logic transitions for data (D), clock (CK), complementary outputs (Q and QB).

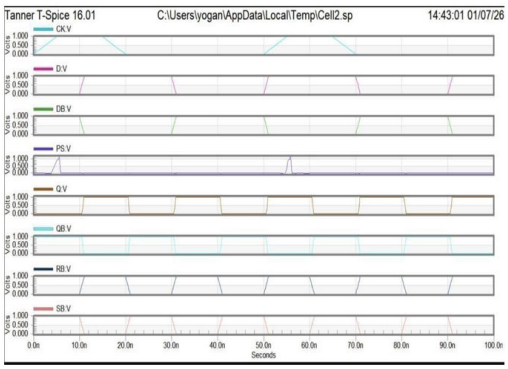


Fig.6:ResultofProposed ConditionalBoosting

The electrical efficiency and timing characteristics are detailed in the measurementsummaries.Thecircuitconsumesa

naveragepowerof$77.89\mu W, with a peak power consumption of 1.07mW occurring at 71 ns. Timing results indicateapropagationdelayof7.08nsforlow-to-hightransitions and4.38nsforhigh- to-low transitions at the Q output, resulting in an average propagation delay (tp_Q_avg)of 5.73 ns in the fig.6These metrics suggest the circuit isoptimized for low- poweroperation with balancedswitchingspeeds.The simulation as shown in fig.6 were highly efficient, completing in approximately0.76to 0.79seconds.The breakdownofsimulationtime showsthatthe DC operating point and Transient Analysis phases were the primary tasks, with the transientphasetakingroughly0.11to0.14seconds.Despitethegenerationof a few warning messages during the setup phase, the status for all runs is marked as "completed" or"finished,"validatingthetimingresultspresented.

VI CONCLUSION

The proposed high-performance boosting flip-flop architecture effectively integrates conditional bridging and conditional boosting techniques to achieve substantial improvements in speed, power efficiency, and reliability for multi-data transmission in low-power VLSI systems. By incorporating explicit pulse control and data-dependent activation mechanisms, the design significantly reduces propagation delay, making it highly suitable for multi-bit pipelined data paths. Implemented and analyzed using 28 nm CMOS technology, the architecture demonstrates notable latency improvement and reduced variability under near-threshold voltage operation. The symmetric differential latch structure enhances noise immunity and ensures zero skew during parallel data transmission, thereby supporting robust high-speed synchronous operation. Simulation results under identical operating conditions confirm that the proposed design achieves a data-to-output delay of 5.73 ns, compared to approximately 18–19 ns in conventional single-ended and differential SAFF architectures, while utilizing only 31 transistors. The average power consumption is maintained at 77.89 µW, resulting in a low energy-delay product across varying switching activities. Although the transistor count is slightly increased, the dramatic enhancement in speed performance validates the effectiveness of the proposed boosting strategy, making it well suited for modern integrated circuits where high-speed and energy-efficient operation are critical design requirements.

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